

What is claimed is:

- 1           1.     A system comprising:  
2           a locked loop circuit; and  
3           a processor coupled to the locked loop circuit to control the locked loop circuit and  
4 perform at least one other function in the system not related to the control of the locked loop  
5 circuit.
- 1           2.     The system of claim 1, wherein the locked loop circuit comprises a delay  
2 locked loop circuit.
- 1           3.     The system of claim 1, wherein the locked loop circuit comprises:  
2 an interface accessible by the processor.
- 1           4.     The system of claim 3, wherein the interface indicates a phase difference  
2 between an input clock signal and an output clock signal generated by the locked loop circuit.
- 1           5.     The system of claim 3, wherein the system comprises a computer system  
2 having a system memory and the interface is addressable in a range of addresses used to  
3 access the system memory.
- 1           6.     The system of claim 3, wherein the interface indicates storage accessible by  
2 the processor to store an indication of a delay used by the locked loop circuit.
- 1           7.     The system of claim 3, wherein the interface includes storage accessible by the  
2 processor to store an indication of a selection of one or more of a plurality of output clock  
3 signals furnished by the locked loop circuit.
- 1           8.     The system of claim 1, wherein the processor comprises a microprocessor.

1 9. The system of claim 1, further comprising:  
2 a system memory storing a program,  
3 wherein the processor executes the program to perform said other function.

1 10. A locked loop circuit comprising:  
2 a delay line to receive an input clock signal and furnish an output clock signal;  
3 a phase detector to indicate a phase difference between the input clock signal and the  
4 output clock signal; and  
5 an interface accessible by a processor to control the locked loop circuit to adjust a  
6 timing between the input clock signal and the output clock signal.

1 11. The locked loop circuit of claim 10, wherein the locked loop circuit comprises  
2 a delay locked loop circuit.

1 12. The locked loop circuit of claim 10, wherein the interface indicates a phase  
2 difference between an incoming clock signal to the locked loop circuit and another signal  
3 generated by the locked loop circuit.

1 13. The locked loop circuit of claim 10, wherein the interface is addressable in a  
2 range of addresses used to access a system memory of a computer system.

1 14. The locked loop circuit of claim 10, wherein the interface includes storage  
2 accessible by the processor to store an indication of a delay applied by the locked loop circuit  
3 to the input clock signal.

1 15. The locked loop circuit of claim 10, wherein the interface includes storage  
2 accessible by the processor to store an indication of a selection of one of a plurality of output  
3 clock signals furnished by the locked loop circuit.

1 16. A method comprising:  
2 providing a locked loop circuit having a processor accessible interface; and  
3 using a processor to control the locked loop circuit and perform at least one other  
4 function not related to the control of the locked loop circuit.

1 17. The method of claim 16, wherein the locked loop circuit comprises a delay  
2 locked loop circuit.

1 18. The method of claim 16, further comprising:  
2 performing at least one of read and write operations to the interface to control the  
3 locked loop circuit.

1 19. The method of claim 16, further comprising:  
2 using the interface to indicate a phase difference between an input clock signal and an  
3 output clock signal generated by the locked loop circuit.

1 20. The method of claim 16, wherein the system comprises a computer system  
2 having a system memory and the interface is addressable in a range of addresses used to  
3 access the system memory.

1 21. The method of claim 16, further comprising:  
2 using the interface to store an indication of a delay used by the locked loop circuit.

1 22. The method of claim 16, further comprising:  
2 using the interface to store an indication of a selection of one or more of a plurality of  
3 output clock signals furnished by the locked loop circuit.

1 23. The method of claim 16, wherein the processor comprises a microprocessor.